

PATENT APPLICATION  
DOCKET NO.: 1285-0080US  
ALC-135942

WHAT IS CLAIMED IS:

1       1. An arbitration system for a network switch  
2 element, comprising:

3               an encoder for encoding a plurality of inputs  
4 into address information associated with a storage  
5 structure, said inputs corresponding to control signals  
6 generated by a plurality of entities associated with a  
7 cross-connect matrix of said network switch element,  
8 wherein said entities are operable to establish a set of  
9 connections through said cross-connect matrix for  
10 transporting data from said network switch element's  
11 ingress side to its egress side;

12              said storage structure including a plurality of  
13 fields for storing pre-computed arbitration results based  
14 on a select arbiter scheme employed in a particular  
15 scheduling mechanism for transporting said data, wherein  
16 each arbitration result corresponds to at least a  
17 particular input combination; and

18              a decoder for decoding a selected arbitration  
19 result into an identity associated with a corresponding  
20 entity.

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1           2. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said storage  
3 structure comprises a look-up table.

1           3. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said storage  
3 structure is realized in a read-only memory (ROM).

1           4. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said storage  
3 structure is realized in an electrically programmable  
4 read-only memory (EPROM).

1           5. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said storage  
3 structure is realized in a dynamic random access memory  
4 (DRAM).

1           6. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said storage  
3 structure is realized in a static random access memory  
4 (SRAM).

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1       7. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said storage  
3 structure is realized in a Flash memory.

1       8. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said storage  
3 structure is realized in a field-programmable gate array  
4 (FPGA).

1       9. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said storage  
3 structure is realized in a application-specific  
4 integrated circuit (ASIC).

1       10. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said select  
3 arbiter scheme includes at least one flexible ring  
4 arbiter.

1       11. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said select  
3 arbiter scheme includes at least one binary tree arbiter  
4 (BTA).

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1       12. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said select  
3 arbiter scheme includes at least one round-robin arbiter  
4 (RRA).

1       13. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said select  
3 arbiter scheme includes at least one fixed priority  
4 arbiter.

1       14. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said select  
3 arbiter scheme is implemented at said network switch  
4 element's ingress side.

1       15. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said select  
3 arbiter scheme is implemented at said network switch  
4 element's egress side.

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1       16. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said arbiter  
3 scheme is implemented as at least one of a request  
4 arbiter, a grant arbiter and an accept arbiter.

1       17. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said arbiter  
3 scheme is implemented as part of a Request-Grant-Accept  
4 (RGA) iteration strategy associated with said particular  
5 scheduling mechanism.

1       18. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said arbiter  
3 scheme is implemented as part of a Request-Grant (RG)  
4 iteration strategy associated with said particular  
5 scheduling mechanism.

1       19. The arbitration system for a network switch  
2 element as set forth in claim 1, wherein said encoder is  
3 operable to encode prior state information associated  
4 with select arbiter scheme into a portion of said address  
5 information, wherein said prior state information is  
6 operable to be updated by said select arbiter scheme in  
7 a predetermined manner.

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1           20. An arbitration methodology for a network switch  
2 element, comprising the steps:

3                 encoding a plurality of inputs into address  
4 information associated with a storage structure, said  
5 inputs corresponding to control signals generated by a  
6 plurality of entities associated with a cross-connect  
7 matrix of said network switch element, wherein said  
8 entities are operable to establish a set of connections  
9 through said cross-connect matrix for transporting data  
10 from said network switch element's ingress side to its  
11 egress side;

12               storing pre-computed arbitration results in a  
13 plurality of fields associated with said storage  
14 structure, wherein said arbitration results are based on  
15 a select arbiter scheme employed in a particular  
16 scheduling mechanism for transporting said data, each  
17 arbitration result corresponding to at least a particular  
18 input combination;

19               responsive to a particular input combination in  
20 an arbitration iteration, obtaining a selected  
21 arbitration result from said storage structure; and

22               decoding said selected arbitration result into  
23 an identity associated with a corresponding selected  
24 entity for said arbitration iteration.

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1           21. The arbitration methodology for a network  
2 switch element as set forth in claim 20, further  
3 comprising the steps:

4                 updating prior state information associated  
5 with said select arbiter scheme in a predetermined manner  
6 based on said arbitration result obtained in an  
7 arbitration iteration; and

8                 utilizing said updated state information as at  
9 least a portion of said address information for a next  
10 arbitration iteration.

1           22. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 pre-computed arbitration results are stored in a look-up  
4 table (LUT).

1        23. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 pre-computed arbitration results are stored in a storage  
4 structure selected from the group consisting of a read-  
5 only memory (ROM) structure, an electrically programmable  
6 read-only memory (EPROM) structure, a dynamic random  
7 access memory (DRAM) structure, a static random access  
8 memory (SRAM) structure, a Flash memory structure, a  
9 field-programmable gate array (FPGA) and an application-  
10 specific integrated circuit (ASIC).

1        24. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 select arbiter scheme includes at least one flexible ring  
4 arbiter.

1        25. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 select arbiter scheme includes at least one binary tree  
4 arbiter (BTA).

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1        26. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 select arbiter scheme includes at least one round-robin  
4 arbiter (RRA).

1        27. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 select arbiter scheme includes at least one fixed  
4 priority arbiter.

1        28. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 select arbiter scheme is implemented at said network  
4 switch element's ingress side.

1        29. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 select arbiter scheme is implemented at said network  
4 switch element's egress side.

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1       30. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 arbiter scheme is implemented as at least one of a  
4 request arbiter, a grant arbiter and an accept arbiter.

1       31. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 arbiter scheme is implemented as part of a Request-Grant-  
4 Accept (RGA) iteration strategy associated with said  
5 particular scheduling mechanism.

1       32. The arbitration methodology for a network  
2 switch element as set forth in claim 20, wherein said  
3 arbiter scheme is implemented as part of a Request-Grant  
4 (RG) iteration strategy associated with said particular  
5 scheduling mechanism.